Amendments to the Drawings:

The attached replacement sheet includes changes to Figs. 4–6. The replacement sheets are respectively submitted in accordance with 37 C.F.R. §§ 1.84 and 1.121.

Attachment: Replacement Sheets (2)

REMARKS

Applicants respectfully traverse and request reconsideration.

Amendments have been made to the written description, the claims and to the drawings. Claims 1, 8–9, 11–12, 17–19, the second instance of claim 22, and claims 23–24 have been amended to clarify the existing subject matter. Thus, it is respectfully submitted that the above amendments are not made for reasons related to patentability. Claim 16 has been cancelled without prejudice. Claim 8 has further been amended to include the subject matter originally presented in claim 16. Claims 26–29 have been added.

The amendments to FIG. 4 correct typographical errors corresponding to reference numerals 162, 164, 165, and 178. The reference label for reference numeral 162 now reads "TILE MINZ," the reference label for reference numeral 164 now reads "TILE MAXZ," and the reference label for reference numeral 165 now reads "XY." Support for this amendment may be found, among other places, in ¶ 0036. FIG. 4 is further amended such that reference numeral 178 references a module entitled "HIERARCHICAL Z BUFFER & STENCIL CACHE UPDATER AND KILL/PASS." Applicants respectfully submit that the aforementioned amendments are consistent with the claims and with at least ¶0037 of the present written description, and thus are not believed to add new subject matter.

The amendment to FIG. 5 corrects method block 206 and specifically replaces the second instance of the term "tile" with the term "tile Z value range." The amendment to FIG. 6 adds the term "tile" after the fourth instance of the article "the" in method block 230.

The drawings stand objected to under 37 C.F.R. § 1.83(a) for allegedly not showing every feature of the invention specified in the claims. Specifically, the present Office Action states that "a hierarchical Z buffer and stencil cache updater must be shown or the feature(s) canceled from the claim(s)." As the Office Action properly noted, a hierarchical update and kill/pass module

178 was previously illustrated in originally submitted FIG. 4. By the above amendment, module 178 is now entitled "HIERARCHICAL Z BUFFER & STENCIL CACHE UPDATER AND KILL/PASS." As indicated, support for this amendment is found in at least in ¶ 0037 where Applicants teach that "the tile hierarchical update and kill/pass module 178 updates the hierarchical cache MinZ, hierarchical cache MaxZ and the stencil codes 180 within the hierarchical Z and stencil cache 144 in response to the comparator 160 …." Applicants note that this amendment is consistent with the claims and the remainder of the present written description. Accordingly, Applicants respectfully submit that the figures are in proper condition and that the objection should be withdrawn.

The second instance of originally submitted claim 22 and originally submitted claims 23–24 stand object to because there are duplicate claims numbered 22. Amendments have been made to correct this typographical error. Accordingly, Applicants respectfully believe that the objection should be withdrawn.

Claims 1–25 stand rejected under 35 U.S.C. § 103(a) as being unpatentable in view of U.S. Patent Publication No. 2005/0134588A1 to Aila et al. ("Aila") in view of U.S. Patent No. 5,579,455 to Greene et al. ("Greene").

Aila is directed to a processor for image processing in accordance with shadow polygons defining together a set of tiles, each tile being formed of a set of pixels and having a respective tile volume defined by the set of pixels and depth values relating to the set of pixels. The processor is further configured to determine whether a tile is a potential boundary tile or a non-boundary tile, a potential boundary tile having a tile volume intersected by at least one of the shadow polygons. (Abstract). If the tile volume is intersected by a shadow volume, a shadow volume algorithm is carried out on a per-pixel level. If, however, the tile volume is not

intersected by a shadow polygon, the shadow volume algorithm is carried out for a point within the tile. If the point is lit, the tile is fully lit; if the point is not lit, the tile is fully in shadow. (FIG. 4).

Greene is directed to rendering of 3D scenes on a display using hierarchical Z-buffer visibility. (See title). A visibility algorithm is used to reject hidden geometry very quickly. (Col. 3, ll. 55–67). A polygon is hidden with respect to a Z-buffer if no pixel of the polygon is closer to the observer than the Z value already in the Z-Buffer. (Col. 4, ll. 14–16). The algorithm employed by Greene incorporates a Z-pyramid that uses a conventional depth buffer (Z-buffer), where at each level a plurality of Z-values are combined into one Z value. "Every entry in the pyramid therefore represents the farthest Z for a square area of the Z-buffer. At the coarsest level of the pyramid there is a single Z value which is the farthest Z from the observer in the whole image." (Col. 5, ll. 51–59). The algorithm recursively goes through multiple levels of the Z-pyramid where at each level, the nearest Z value of the primitive is compared to that level's Z value in the Z-pyramid. If the Z-pyramid value is closer, the primitive is hidden in the quadrant. (Col. 6, ll. 19–37). In one embodiment, Greene mentions that a Z-max value and a Z-min value may be compared to the nearest value of the primitive. (Col. 17, ll. 23–40). However, in each case, the Z-max value and the z-min value of the Z-pyramid are always compared to the same z-value of the primitive (i.e., the z-value representing the nearest depth of the primitive). (Col. 17, ll. 25–30, 34–37).

As to claim 1, Applicants claim, among other things, "comparing a tile Z value range with a hierarchical Z value range and a stencil code." Because no combination of Aila or Greene teaches or suggests this limitation, claims 1 and 8 are believed to be in proper condition for allowance. Further, Applicants note that the Office Action is silent as to the claimed "updating

the hierarchical Z value range and the stencil code in response thereto." For at least the reason that the Office Action does not address each and every claim limitation, claim 1 is believed to be allowable over the cited prior art.

Specifically, the Office Action states that Aila fails to explicitly teach a hierarchical Z value range. The Office Action then alleges that Greene teaches this feature of the claims. At no point, however, does any combination of Aila and Greene teach, suggest or otherwise disclose comparing a tile Z value range with a hierarchical Z value range. Turning first to Aila, Applicants submit that the Office Action appears to correctly identify the omission of any teaching, suggestion or disclosure of a hierarchical Z value range. At best, Aila appears to teach comparing a tile Z min or a tile Z max value with a single representative Z value and not a hierarchical Z value range as claimed. Although Greene appears to teach a Z-pyramid Z-min and Z-max value, Greene also compares each of the Z-min value and the Z-max value with a single representative z-value of a given primitive (i.e., the z-value representing the nearest depth of the primitive). (Col. 17, ll. 25–30, 34–37). Because each of the references purportedly disclose comparing a single Z value to a range and do not appear to provide any teaching, suggestion or other disclosure comparing a tile Z value range with a hierarchical Z value range and a stencil code as claimed, Applicants respectfully believe claim 1 to be in condition for allowance.

Moreover, Applicants respectfully submit that the Office Action has failed to provide a proper motivation to combine Alia with Greene. At best, Aila and Greene appear to practice the prior art as articulated by Applicants in the Background of the Application. Therein, Applicants teach that "conventional video graphics circuits cannot perform both hierarchical z-buffering and stencil operations because the circuit must choose to perform either the hierarchical z-buffering or the buffering. The hierarchical Z-buffering is typically disabled during the stencil test because

the stencil test interacts with Z buffering operation[s]. Therefore, without a means of performing a hierarchical stencil test, it is generally impossible to know the correct result for a hierarchical depth test." (Applicants' specification, ¶0009). As admitted by the Office Action, Aila fails to teach a hierarchical Z value range and thus does not teach hierarchical Z buffering as disclosed by Applicants. In the same vein, Applicants can find no reference in Greene as to the claimed stencil code (*see e.g.,* claim 1) or the claimed stencil test (*see e.g.,* claim 2). Thus, for argument's sake, even if Aila taught the claimed features of the stencil code and even if Greene taught a hierarchical Z value range or hierarchical z-buffering, they would individually only practice the prior art and perform as conventional video graphics circuits. Because conventional video graphics circuits suffer from not having "a means of performing a hierarchical stencil test" and thus "it is in general impossible to know the correct result for a hierarchical depth test," Applicants respectfully submit that the alleged motivation to combine Aila and Greene is improper; without Applicants' disclosure, one having ordinary skill in the art would not be motivated to combine the teachings of Aila and Greene. As the Office Action appears to rely on improper hindsight when it states that one would be motivated to combine Aila with Green to achieve increased processing speed, Applicants submit that a *prima facie* case of obviousness has not been established. For this reason alone, claim 1 is believed to be in proper condition for allowance.

Claims 2–7 depend upon allowable claim 1 and further contain additional novel and non-obvious subject matter. Applicants further submit that the Office Action fails to address claim language in the rejection of at least claim 3 where it states that "the rationale disclosed in the rejection of claim 2 is incorporated herein." Applicants respectfully note that the claim language of claim 3 is different than the language of claim 2 and thus cannot be addressed by merely

pointing to the rationale made with respect to claim 2. For at least these reasons, claim 2–7 are further believed to be in proper condition for allowance over Aila and Greene.

As to claim 8, Applicants respectfully submit that the Office Action fails to address the claim language presented by Applicants. For instance, on page 6, ¶12, the Office Action states that "In regards to claim 8 the rationale disclosed in the rejection of claim 1 is incorporated herein." Applicants however respectfully note that the claim language of claim 1 is different than the claim language of claim 8 and, therefore, the scope of claim 1 is different than the scope of claim 8. For this reason alone, claim 8 is believed to be allowable over the cited prior art.

Moreover, Applicants respectfully submit that claim 8 is allowable because no combination of the cited portions of Aila or Greene appear to teach, suggest or otherwise disclose the claimed "updating a hierarchical Z value range and a stencil code in response thereto." Similarly, Applicants further reassert the relevant remarks made above with respect to claim 1 and note that the Office Action has failed to provide a proper motivation to combine Aila and Greene. Accordingly, claim 8 is further believed to be allowable over the cited prior art.

Claims 9–15 depend upon allowable claim 8 and further contain additional novel and non-obvious subject matter. For at least these reasons, claim 9–15 are further believed to be in proper condition for allowance over Aila and Greene.

As to claim 17, Applicants claim a comparator, a hierarchical Z buffer and stencil cache operably coupled to the comparator; and a hierarchical Z buffer and stencil cache updater operably coupled to the comparator wherein the hierarchical Z buffer and stencil cache provides a cache MinZ, a cache MaxZ, and a stencil code to the comparator. The Office Action asserts that the claimed comparator is allegedly taught by the CPU (element 501) of Aila's FIG. 5, that the hierarchical Z buffer is allegedly taught by the depth buffer (element 521) of Aila's FIG. 5

and the memory (element 104) of Greene's FIG. 1, the stencil cache is allegedly taught by the stencil buffer (element 523) of Aila's FIG. 5, and the hierarchical Z buffer and stencil cache updater is allegedly taught by the graphics processor (element 510) of Aila's FIG. 5. Applicants respectfully submit that the above allegations fail to address each and every limitation of the current claim and therefore fails to render obvious Applicants' claimed subject matter.

Applicants first note that claim 17 features, among other things, a hierarchical Z buffer and stencil cache that provides a cache MinZ, a cache MaxZ, and a stencil code to a comparator. Applicants respectfully note that the present Office Action fails to address this claim limitation. For this reason alone, Applicants respectfully submit that a *prima facie* case of obviousness has not been provided and the claims are in proper condition for allowance. For argument's sake, however, the Office Action's recitation of individual features of Aila and Greene are inconsistent with this particular claim feature. For instance, the present Office Action states that the CPU (element 510) is allegedly analogous to Applicants' comparator while the depth buffer (element 521) and stencil buffer (element 523) are allegedly analogous to Applicants' hierarchical Z buffer and stencil cache. Applicants respectfully submit that these statements are improper given that Aila's depth buffer and stencil buffer (elements 521 and 523) do not appear to provide a cache MinZ, cache MaxZ and a stencil code to the CPU (element 501). Applicants support this contention by drawing the Examiner's attention to the illustration provided in Aila's FIG. 5 where CPU (element 501) is illustrated without input from any source. Accordingly, Applicants respectfully submit that claim 17 is in proper condition for allowance.

Applicants also reassert the relevant remarks made above with respect to claim 1 and note that the Office Action has failed to provide a proper motivation to combine the teachings of Aila

and Greene. For this reason alone, claim 17 is further believed to be allowable over the cited prior art.

Claims 18–22 depend upon allowable claim 17 and further contain additional novel and non-obvious subject matter. For at least these reasons, claims 18–22 are believed to be in proper condition for allowance.

As to claim 23, Applicants respectfully reassert the relevant remarks made above with respect to claims 1 and 17. Because claim 23 features, among other things, a hierarchical Z buffer and stencil cache and comparator as claimed in claim 17 and because claim 23 further features comparing the tile MinZ and the tile MaxZ to the cache MinZ, the cache MaxZ, and the stencil code, Applicants respectfully assert that claim 23 is in proper condition for allowance for at least the same reasons articulated above.

Claims 24–25 depend upon allowable claim 23 and further contain additional novel and non-obvious subject matter. For at least these reasons, claims 24–25 are believed to be in proper condition for allowance.

New claim 26 depends upon allowable claim 1 and further contains additional novel and non-obvious subject matter. For instance, claim 26 provides that comparing a tile Z value range with a hierarchical Z value range and a stencil code comprises comparing the stencil code to a stencil value and a stencil mask. For at least these reasons, claim 26 is also believed to be in proper condition for allowance.

New claim 27 includes "determining if a tile is visible relative to a stencil by generating a stencil code and comparing the stencil code to a stencil value and a stencil mask." Applicants can find no teach or suggestion of this limitation in the cited portions of the prior art. For this reason alone, claim 27 is believed to be allowable over the cited prior art. Similarly, new claim 27

includes "determining if the tile is visible in a hierarchical Z plane by comparing a MinZ and a MaxZ for the tile to a hierarchical Z range." Because each of the references purportedly disclose comparing a single Z value to a range and do not appear to provide any teaching, suggestion or other disclosure comparing a MinZ and a MaxZ for the tile to a hierarchical Z value range, as claimed, Applicants respectfully believe claim 27 to be in condition for allowance. Applicants further and respectfully reassert the relevant remarks made above with respect to claim 1 and note that the purported motivation to combine Aila and Greene is improper. Thus, claim 27 is believed to be allowable over the cited prior art for this reason as well as those articulated above.

New claims 28–29 depend upon allowable claim 27 and further contains additional novel and non-obvious subject matter. For at least these reasons, claim 28–29 are further believed to be in proper condition for allowance over Aila and Greene.

Applicants respectfully submit that the claims are in condition for allowance and respectfully request that a timely Notice of Allowance be issued in this case. The Examiner is invited to contact the below listed attorney if the Examiner believes that a telephone conference will advance the prosecution of this application.

Respectfully submitted,

Date: 10/4/06

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